**Simulation Results: Analog Entropy Override Controller (analog\_entropy\_waveform\_log.png)**

This document presents the key waveforms obtained from the time-domain (transient) simulation of the analog\_entropy\_override\_stage.asc circuit. The plot effectively demonstrates the circuit's intended hazard response logic based on analog entropy, noise, and an ML override trigger.

**1. Plot Overview**

The provided waveform plot displays the following signals over a 1 millisecond (1ms) simulation period:

* **Green Trace:** V\_entropy (Input) - Represents the simulated entropy score.
* **Red Trace:** V\_noise (Input) - Represents the analog interference or chaos signal.
* **Yellow Trace:** V\_ml\_trigger (Input) - Represents the digital ML override activation.
* **Cyan Trace:** LOCK\_OUT (Output) - The logic high signal indicating a lockout condition.
* **Magenta Trace:** FLUSH\_OUT (Output) - The short pulse indicating a chaos surge.

Two horizontal dashed lines are also visible, indicating key threshold voltages: 3.3V (for entropy comparison) and 2.0V (for noise comparison).

**2. Analysis of Waveforms**

**V\_entropy (Input) - Green Trace**

* **Behavior:** This trace shows a clear, linear ramp-up from 0V at 0ms to 5V at 1ms.
* **Interpretation:** This confirms the correct setup of the PWL source for V\_entropy, accurately simulating a steadily increasing entropy score over the observed period.

**V\_noise (Input) - Red Trace**

* **Behavior:** The V\_noise trace displays sharp, distinct positive spikes, reaching approximately 2.5V. These spikes occur precisely at 0.2ms, 0.4ms, 0.6ms, and 0.8ms. Each spike is very narrow, lasting for a short duration.
* **Interpretation:** This verifies the accurate generation of the simulated chaos signal, designed to inject momentary, high-amplitude interference.

**V\_ml\_trigger (Input) - Yellow Trace**

* **Behavior:** The V\_ml\_trigger trace remains at 0V until 0.5ms. At this point, it sharply transitions to 1V and remains at this logic high level for the remainder of the simulation.
* **Interpretation:** This confirms the precise timing of the ML override activation, which is critical for the conditional LOCK\_OUT logic.

**LOCK\_OUT (Output) - Cyan Trace**

* **Behavior:** The LOCK\_OUT signal remains at 0V until approximately 0.66ms. At this point, it transitions sharply to 1V and stays high until the end of the simulation.
* **Interpretation:** This behavior perfectly matches the design specification:
  + V\_ml\_trigger goes high at 0.5ms.
  + V\_entropy (green trace) crosses the 3.3V threshold line at approximately 0.66ms.
  + The LOCK\_OUT condition (V\_entropy > 3.3V AND V\_ml\_trigger = 1V) is met when both input conditions are simultaneously high, which is from 0.66ms onwards. The output correctly reflects this logical AND operation.

**FLUSH\_OUT (Output) - Magenta Trace**

* **Behavior:** The FLUSH\_OUT signal displays very short, active-high (1V) pulses. These pulses coincide precisely with the peaks of the V\_noise (red trace) spikes, occurring at 0.2ms, 0.4ms, 0.6ms, and 0.8ms. The pulses are brief, quickly returning to 0V between noise events.
* **Interpretation:** This confirms the successful detection and translation of V\_noise surges. The circuit accurately generates a reactive "flush" pulse each time the V\_noise exceeds its 2V threshold, demonstrating the differentiator and logic's ability to capture transient chaotic events.

**3. Conclusion**

The simulation results conclusively demonstrate that the LTSpice Analog Entropy Override Controller prototype functions precisely as designed. Both the LOCK\_OUT and FLUSH\_OUT logic paths exhibit the expected responses to their respective input conditions. This successful prototype build provides a robust foundation for further development and integration within the broader hazard response system described in Paper 5.